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(54) **MULTI-DIE SEMICONDUCTOR PACKAGE**

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(51) **Int. Cl.**

H01L 23/495	(2006.01)
H01L 23/31	(2006.01)
H01L 23/00	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 23/49562*** (2013.01); ***H01L 23/3171*** (2013.01); ***H01L 23/49575*** (2013.01); ***H01L 24/32*** (2013.01); *H01L 24/06* (2013.01); *H01L 24/29* (2013.01); *H01L 24/45* (2013.01); *H01L 24/48* (2013.01); *H01L 24/49* (2013.01); *H01L 24/83* (2013.01); *H01L 2224/02166* (2013.01); *H01L 2224/04026* (2013.01); *H01L 2224/04042* (2013.01); *H01L 2224/0603* (2013.01); *H01L 2224/06181* (2013.01);

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(58) **Field of Classification Search**

None

See application file for complete search history.

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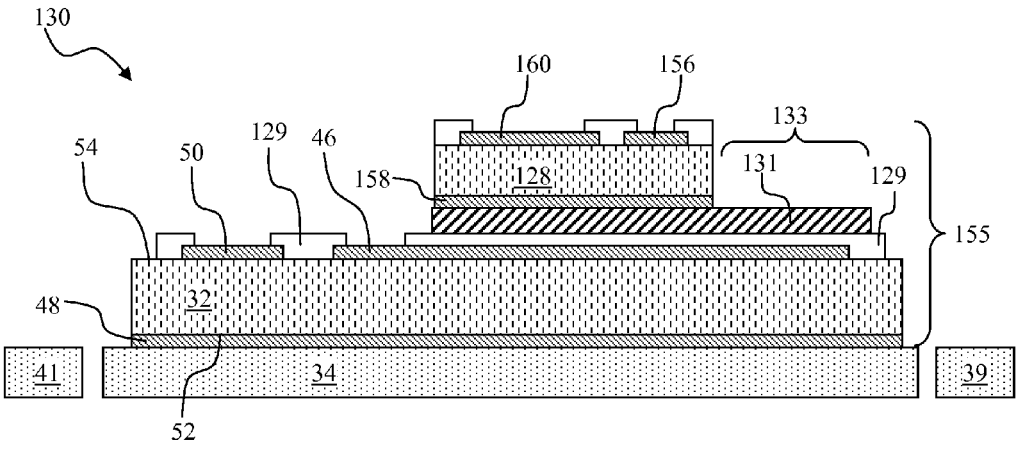
(57) **ABSTRACT**

A multi-die package has a plurality of leads and first and second semiconductor dies in superimposition and bonded together defining a die stack. The die stack has opposed first and second sides, with each of the first and second semiconductor dies having gate, drain and source regions, and gate, drain and source contacts. The first opposed side has the drain contact of the second semiconductor die, which is in electrical communication with a first set of the plurality of leads. The gate, drain and source contacts of the first semiconductor die and the gate and source contacts of the second semiconductor die are disposed on the second of said opposed sides and in electrical communication with a second set of the plurality of leads. The lead for the source of the first semiconductor die may be the same as the lead for the drain of the second semiconductor die.

17 Claims, 5 Drawing Sheets



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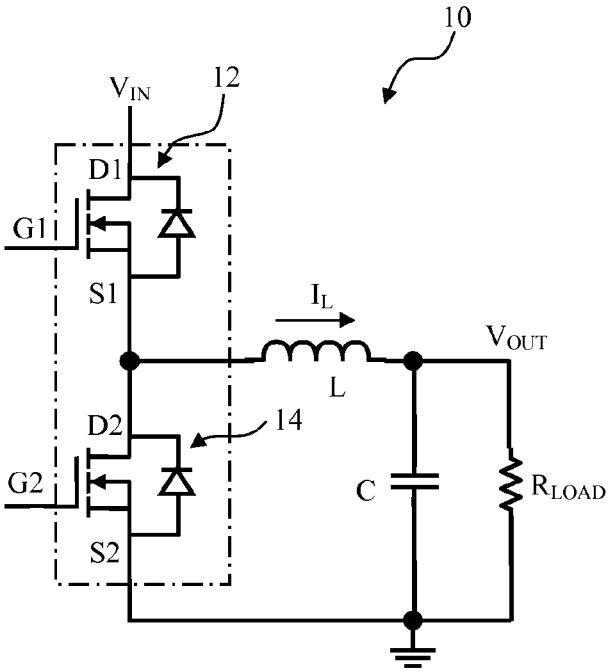

Fig. 1 Prior Art

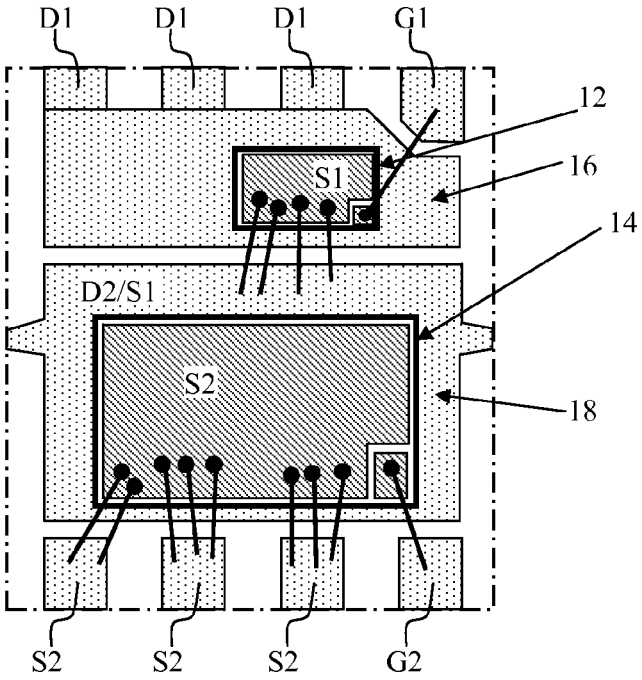

Fig. 2 Prior Art

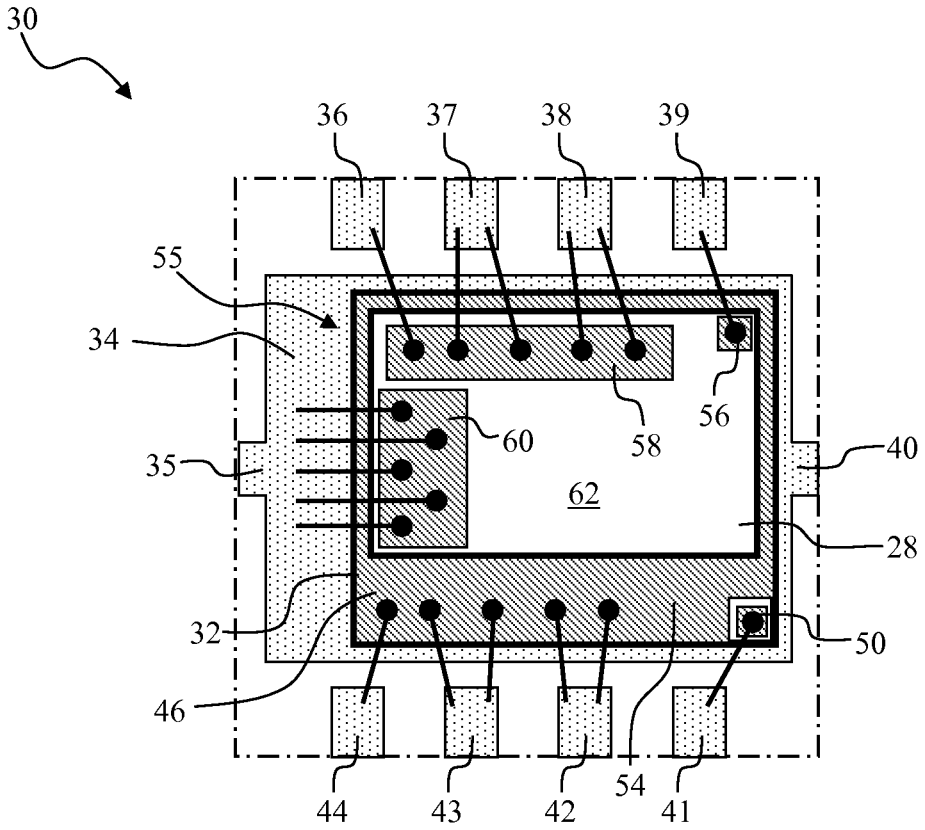

Fig. 3

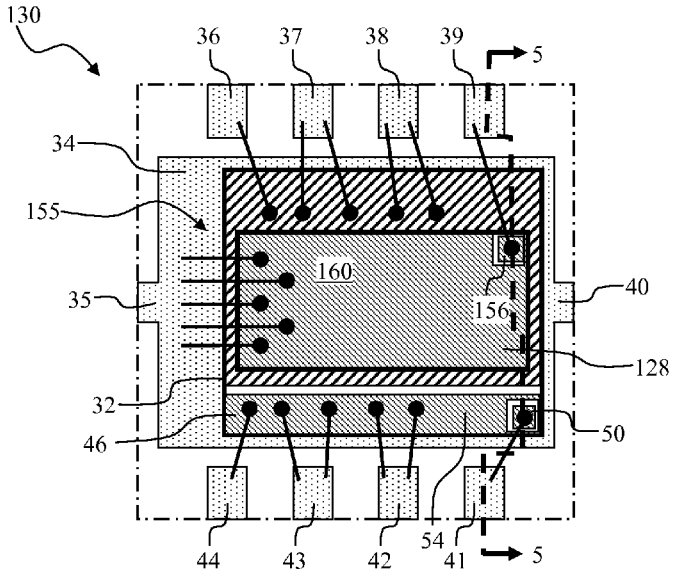
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Fig. 4

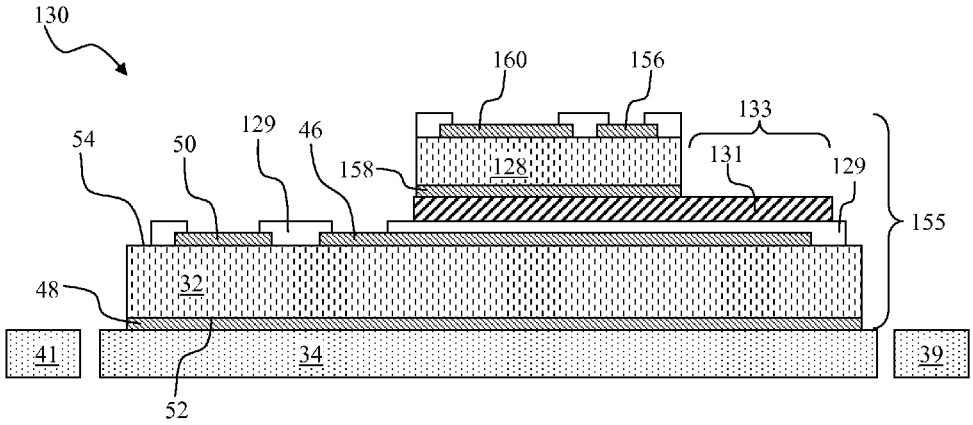
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Fig. 5

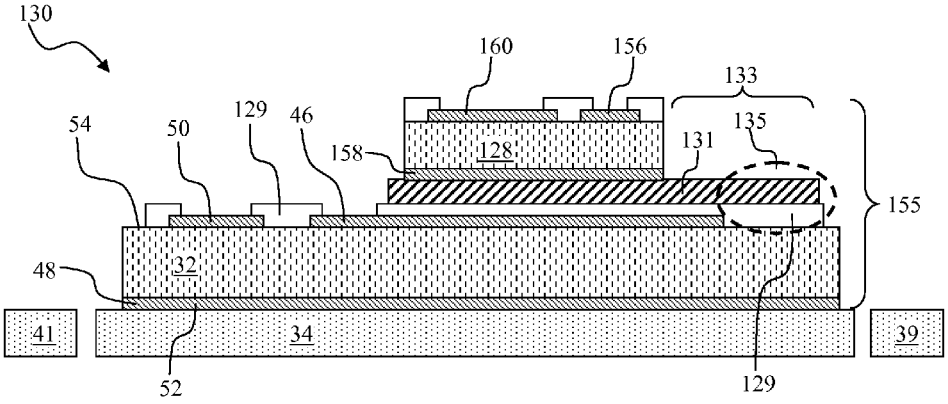

Fig. 6

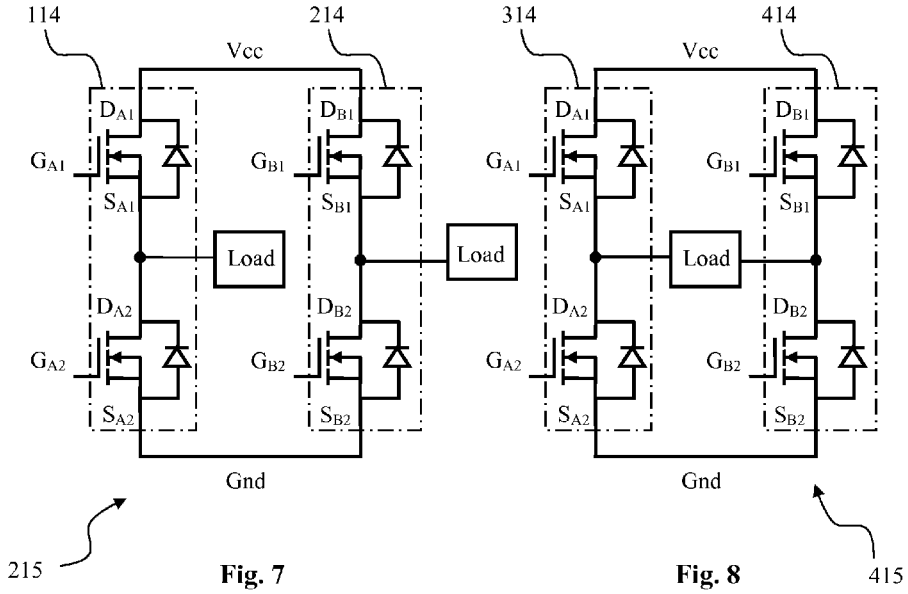

Fig. 7

Fig. 8

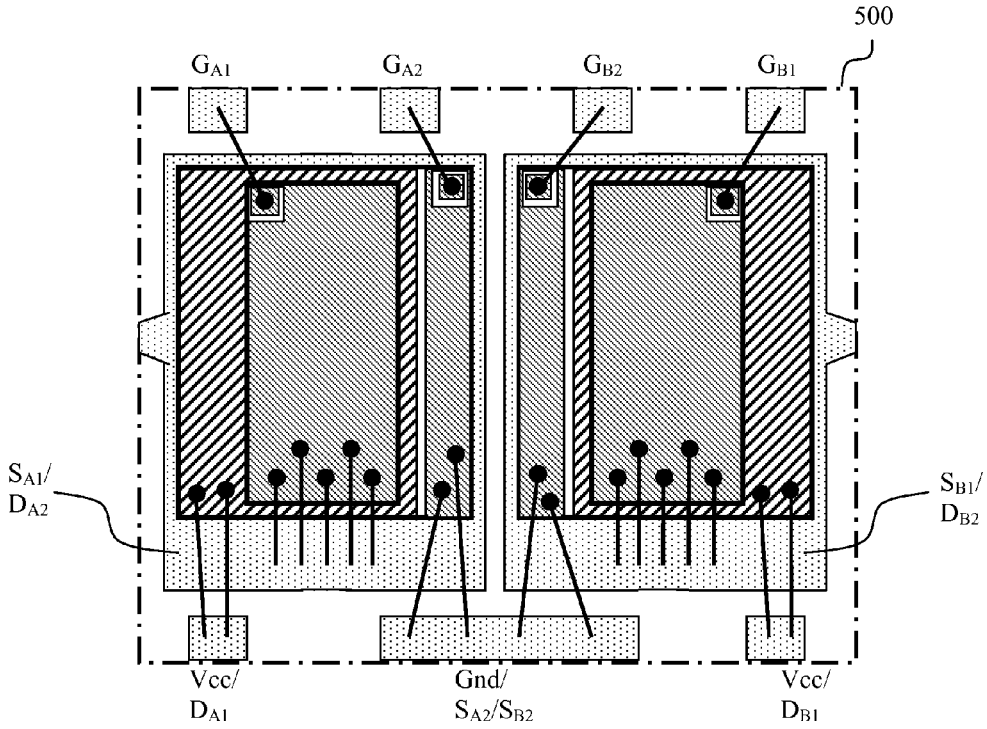

Fig. 9

MULTI-DIE SEMICONDUCTOR PACKAGE

The instant application claims priority to and is a continuation application of U.S. patent application Ser. No. 12/534,057 (now U.S. Pat. No. 8,164,199) titled "Multi-die package", filed on Jul. 31, 2009.

BACKGROUND OF THE INVENTION

The present invention generally relates to semiconductor packages and more particularly to semiconductor packages and methods of making semiconductor packages.

In many MOSFET switching circuits a pair of power MOSFETs is switched in complementary fashion. A typical MOSFET switching circuit **10** is shown in FIG. **1** and includes two MOSFETs **12** and **14** coupled in series across a voltage source V_{in} and ground. MOSFETs **12** and **14** are typically referred to as high side and low side MOSFETs, respectively.

To initiate a switching cycle, MOSFET **14** is first turned off. As a result, the body diode of MOSFET **14** turns-on and drives current. After a delay, MOSFET **12** turns on, turning-off the body diode of MOSFET **14**. This generates a recovery current I_L through, as well as, trace inductances (not shown) associated with switching circuit **10**, producing oscillations.

In order to save space and cost, MOSFETs **12** and **14** are often co-packaged together, as indicated by a dashed line. It is the goal of MOSFETs **12** and **14** to attain the highest power density possible in order to work efficiently. The power density is closely related to the die area, i.e., the larger the die, the lower the drain-to-source on resistance, Rdson. Typically, MOSFETs **12** and **14** are co-packaged side by side, on separate die pads, as shown in FIG. **2**. The overall package outline is indicated by the dashed line. Conventional power MOSFETs **12** and **14** are vertical devices, with the source S**1** and S**2**, respectively, and gate, G**1** and G**2**, respectively, on one side, and the drain, D**1** and D**2**, respectively, on an opposing side. MOSFET **12** is attached to a die pad **16**, which has leads extending from it allowing connection to drain D**1**. MOSFET **14** is attached to a die pad **18**. The low side die pad can be exposed through the bottom of a dual flat non-leaded (DFN) package for external connection to drain D**2** and source S**1**. Typically low side MOSFET **14** has a larger die area, compared to high side MOSFET **12**, because MOSFET **14** is usually turned on for a longer duration of time. Source S**1** contacts drain D**2** by way of bond wires from S**1** to die pad **18**. Gates G**1** and G**2**, as well as source S**2** are connected to the appropriate leads by bond wires. The die areas of MOSFETs **12** and **14** are constrained by the package size and by the side by side configuration of the dies.

Therefore, a need exists to improve the operational performance by maximizing the die area of MOSFETs to minimize Rdson without unduly increasing the overall size of the circuit.

SUMMARY OF THE INVENTION

In accordance with one aspect of the invention, a multi-die package has a plurality of leads and comprises first and second semiconductor dies in superimposition and bonded together defining a die stack. The die stack has opposed first and second sides, with each of the first and second semiconductor dies having gate, drain and source regions, and gate, drain and source contacts. The first opposed side has the drain contact of the second semiconductor die, which is in electrical communication with a first set of the plurality of leads. The gate, drain and source contacts of the first semiconductor die and the gate and source contacts of the second semiconductor die are disposed on the second of the opposed sides so as to be present in different planes, and in electrical communication with a second set of the plurality of leads. With this configuration, the die area of first and second semiconductor dies may be maximized without unduly increasing the overall size of the circuit. In accordance with another embodiment of the present invention, a floating metal layer may be disposed upon one of the first and second semiconductor dies to function as both a die pad and a bonding pad for the remaining semiconductor die of the first and second semiconductor dies. These and other aspects of the invention are discussed more fully below.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram of a MOSFET switching circuit in accordance with the prior art;

FIG. **2** is a top down plan view of a multi-chip package in accordance with the prior art;

FIG. **3** is a top down plan view of a multi-chip package in accordance with one embodiment of the present invention;

FIG. **4** is a top down plan view of a multi-chip package in accordance with a second embodiment of the present invention;

FIG. **5** is a cross-sectional view of the multi-chip package in FIG. **4** take along lines **5**-**5**;

FIG. **6** is a cross-sectional view of the multi-chip package shown in FIG. **5**, in accordance with an alternate embodiment;

FIG. **7** is a schematic circuit diagram showing a circuit that may be formed using the present invention;

FIG. **8** is schematic circuit diagram of a full bridge circuit that may be formed using the present invention; and

FIG. **9** is a top down plan view of a multi-chip package in accordance with another embodiment of the present invention that may be employed to form the circuits shown in FIGS. **7** and **8**.

DETAILED DESCRIPTION OF THE INVENTION

Referring to both FIGS. **1** and **3**, one embodiment of the present invention includes a multi-die package **30** in which MOSFET switching circuit **10** is provided. To that end, a first **28** and second **32** semiconductor dies are included. The outline of the semiconductor package **30** is indicated by the dashed line. Second semiconductor die **32** is attached to a die bonding pad **34** of a housing (not shown) that includes a plurality of tie bars **35** and **40**, as well as leads **36**-**39** and **41**-**44**. Semiconductor die **32** includes a MOSFET having gate, drain and source regions (not shown), each of which includes a contact, defining a gate contact **50**, a drain contact (on its bottom surface, not shown), and a source contact **46**. Drain contact is disposed upon a surface (not shown) of semiconductor die **32** that is positioned opposite to a surface **54** upon which gate contact **50** and source contact **46** are positioned. Electrical connection to the drain of semiconductor die **32** is achieved through bonding pad **34**. In this package type, the bonding pad **34** may act as a lead itself, though one exposed at the bottom of the package. To that end, conductive adhesive (not shown), e.g., solder, conductive epoxy, eutectic metals, etc., is used to fixedly position semiconductor die **32** to bonding pad **34**. Source contact **46** is placed in electrical communication with leads **42**-**44** with any known electrical connection technique including clips, plates, ribbons and the like. In the present example, wire bonds are employed, which may be aluminum, gold, copper and the like. Gate contact **50** is in electrical communication with lead **41** with a wire bond.

Alternatively, instead of wire bonds, other suitable interconnections may be used, such as clips, plates, or conductive ribbons.

First semiconductor die **28** is in superimposition with second semiconductor die **32** and bonded thereto using non-conductive attachment substance (not shown), e.g., non-conductive epoxy, forming a die stack **55**. First semiconductor die **28** includes a MOSFET having gate, drain and source regions (not shown), each of which includes a contact, defining a gate contact **56**, a drain contact **58**, and a source contact **60**. Gate contact **56**, drain contact **58**, and source contact **60** are disposed upon a common surface **62** of first semiconductor die **28** that faces away from second semiconductor die **32**. The region of second semiconductor die **32** upon which first semiconductor die **28** is bonded is spaced-apart from both gate contact **50** and the bonding area of source contact **46** to facilitate placement of bonding wires thereto. To that end, a die area of second semiconductor die **32** is greater than a die area of first semiconductor die **28**. Source contact **60** is in electrical communication with drain contact (not shown) of the second semiconductor die **32** by bonding wires extending between bonding pad **34** and source contact **60**. Drain contact **58** is in electrical communication with leads **36-38** and gate contact **56** is in electrical communication with lead **39**, using bonding wires. By placing first **28** and second **32** semiconductor dies in superimposition, the die areas can be maximized.

Semiconductor dies **28** and **32** may include a variety of MOSFETs, such as both N-channel, both P-channel, or of complementary polarity. The MOSFET die parameters may be identical or asymmetrical in nature and optimized for high and low side switching. Second semiconductor die **32** may further include an integrated Schottky rectifier for further performance enhancement. Die stack **55** may be encapsulated in various plastic molds (not shown) and used with various lead frames to form conventional packages including the D-PAK, D2-Pak, multi lead TO-220, DFN or any other package design. The stacked die configuration clearly allows for larger die areas to be attained within the same semiconductor package size which leads to lower Rdson. Lower Rdson can be achieved for the same package footprint area. Alternatively a smaller package can be used while still achieving the same or better Rdson.

Referring to both FIGS. **4** and **5**, in an alternate embodiment, multi-die package **130** includes a first **128** and second **32** semiconductor dies. Second semiconductor die **32** is attached to a die bonding pad **34**, as discussed above. Specifically, conductive adhesive (not shown) is used to fixedly position second semiconductor die **32** to bonding pad **34** of a housing (not shown) that includes a plurality of leads **35-44**. Semiconductor die **32** includes a MOSFET having gate, drain and source regions (not shown), each of which includes a contact, defining a gate contact **50**, a drain contact **48**, and a source contact **46**. Drain contact **48** is disposed upon a surface **52** of semiconductor die **32** that is positioned opposite to a surface **54** upon which gate contact **50** and source contact **46** are positioned. Electrical communication between leads **35** and **40** and drain **48** is achieved through bonding pad **34**. Source contact **46** is placed in electrical communication with leads **42-44** with wire bonds, which may be aluminum, gold, copper and the like. Gate contact **50** is in electrical communication with lead **41** with a wire bond.

First semiconductor die **128** is in superimposition with second semiconductor die **32** and bonded thereto using conductive adhesive (not shown) forming a die stack **155**. First semiconductor die **128** is a MOSFET having gate, drain and source regions (not shown), each have a corresponding contact, defining a gate contact **156**, a drain contact **158** and a source contact **160**. Drain contact **158** is disposed upon a surface of first semiconductor die **128** that is disposed opposite to the surface upon which gate **156** and source **160** contacts are disposed. Drain contact **158** is positioned facing second semiconductor die **32** and in superimposition with source contact **46**. Drain contact **158** is electrically isolated from source contact **46** by the presence of a passivation layer **129** positioned upon source contact **46**. The passivation material employed for passivation layer **129** should be able to withstand the voltage difference between the drain of the first semiconductor die **128** and the source of second semiconductor die **32**. To facilitate electrical communication between lead **36-38** and drain contact **158**, the second semiconductor die **32** further comprises a layer **131** of conductive material, e.g. a floating metal layer, located over passivation layer **129**.

Dimensions of layer **131** are established so that first semiconductor die **128** is in superimposition with a sub-portion of layer **131**, with a remaining region **133** not in superimposition with first semiconductor die **128** having dimensions suitable to facilitate wire bonding thereto. Thus, layer **131** acts as both a die pad for the bottom electrode (e.g., drain contact **158**) of first semiconductor die **128** and a bonding pad for conductive interconnections such as bonding wires to attach to for connection to the bottom electrode, while being insulated from the second semiconductor die **32**. The bond wires are not shown in the cross section of FIG. **4** to avoid obscuring the details. Gate **50** and source **46** contacts may optionally also have a layer of conductive material on top of them (not shown) to bring the tops of the contact areas co-planar with the top of conductive layer **131** and to allow easier contact to the gate and source. Gate contact **156** is in electrical communication with lead **39** and source contact **160** is in electrical communication with die pad **34** in the manner discussed above in FIG. **3** with respect to gate contact **56** and source contact **60**, respectively. The multi-die package **130** has the same advantages as the multi-die package **30** of FIG. **3** of larger die areas and lower Rdson. However the multi-die package **130** has the additional advantage of using standard vertical MOSFETs for the high side MOSFET **128** and low side **32** MOSFET, with source and gate on the top, and drain on the bottom.

Referring to FIG. **6**, it was determined to be beneficial in certain instances to omit portions of source contact **46** in superimposition with a portion **135** of region **133** in which a wire bond would be placed. It was found that with certain metals used as source contact **46**, the structural integrity of passivation layer **129** would become compromised and crack, causing shorts between layer **131** and source contact **46**. If a metal making up source contact **46** is a soft material that is easily deformed, e.g., aluminum, the force of the wire bonding process on layer **131** directly above the source contact **46** could cause the passivation layer in between to crack. To reduce, if not avoid the aforementioned problem, the wire bonding to layer **131** takes place in a portion **135** of layer **131** which does not have source metal **46** directly under it. Setting aside a portion of the second semiconductor die **32** without the source metal **46** on it for wire bonding may sacrifice a small portion of the active area, but results in a more robust semiconductor package and higher manufacturing yields.

Referring to both FIG. **7**, one application of the present invention may be employed to configure two pairs of MOSFETs **114** and **214** in parallel, as the circuit **215**. However, pairs **314** and **414** of MOSFETs may be configured so that each is connected to a common load, shown in FIG. **8** as the full bridge circuit **415**. Either circuit **215** or **415**, shown in FIGS. **7** and **8**, respectively, may be configured as package

500 using two of the die stacks disclosed in this application, as shown in FIG. 9. The leads Vcc/D_{A1} and Vcc/D_{B1} may be connected together externally from the package 500.

It should be understood that the foregoing description is merely an example of the invention and that modifications and may be made thereto without departing from the spirit and scope of the invention and should not be construed as limiting the scope of the invention. For example, thin wafers may be used for the high side and low side MOSFETs in order to keep the package thickness small. Therefore, the scope of the invention should be determined with respect to the appended claims, including the full scope of equivalents thereof.

The invention claimed is:

1. A multi-die package having a plurality of leads, comprising:

first and second semiconductor dies being in superimposition and bonded together defining a die stack having opposed first and second sides, with each of said first and second semiconductor dies having gate, drain and source regions, and gate, drain and source contacts, with said first opposed side having said drain contact of said second semiconductor die, which is in electrical communication with a first set of said plurality of leads, with said gate, drain and source contacts of said first semiconductor die and said gate and source contacts of said second semiconductor die being disposed on said second of said opposed sides and in electrical communication with a second set of said plurality of leads, wherein said source contact of the first semiconductor die is in electrical communication with said drain contact of said second semiconductor die.

2. The package as recited in claim 1, wherein said second side includes first and second spaced-apart surfaces, with said first surface including a conductive metal layer disposed upon said second semiconductor die, with a drain contact of said first semiconductor die facing said first surface and contacting said conductive metal layer, with electrically non-conductive material extending between said second semiconductor die and said conductive metal layer and isolating said second semiconductor die from said conductive metal layer.

3. The package as recited in claim 1, wherein said second side includes first and second spaced-apart surfaces, with said first surface including a conductive metal layer disposed upon said second semiconductor die, with a drain contact of said first semiconductor die being in superimposition with and contacting a first portion of said conductive metal layer with a second portion of said conductive metal layer being in juxtaposition with said first portion, with electrically non-conductive material extending between said second semiconductor die and said conductive metal layer, wherein said second portion is a bonding pad for conductive interconnections.

4. The package as recited in claim 1, wherein said second side includes a surface of said second semiconductor die and a first surface of said first semiconductor die facing away from said surface of said second semiconductor die, with the gate, drain and source contacts of said first semiconductor die lying in said first surface of said first semiconductor die, wherein said first semiconductor die is non-conductively attached to said surface of second semiconductor die.

5. The package as recited in claim 1, wherein said second semiconductor die has an area associated therewith that is greater than an area of said first semiconductor die.

6. A die stack comprising:

a bottom die;

a top die stacked on the bottom die;

a metal layer disposed upon the bottom die, the metal layer being isolated from the bottom die by insulating material, wherein the metal layer acts as an electrically conductive die pad for the top die and as a bond pad for conductive interconnections; and

wherein the bottom die is a first MOSFET having a source on its top and a drain on its bottom, wherein the metal layer is isolated from said source of said first MOSFET by insulating material, and the top die is a second MOSFET having a source disposed upon one side and a drain disposed on a side opposite to said one side and contacting said metal layer.

7. The die stack of claim 6, wherein both the bottom die and the top die are discrete semiconductor devices.

8. The die stack of claim 7, further comprising a lead frame die pad wherein the drain of the bottom die is attached to the lead frame die pad and the source of the top die is connected to said lead frame die pad by conductive interconnections.

9. The die stack of claim 8, further comprising lead frame leads; and

a first set of conductive interconnections connected between a bond pad portion of said metal layer and

a first set of said lead frame leads.

10. The die stack of claim 9, wherein said bottom die is a low side MOSFET, and said top die is a high side MOSFET.

11. The die stack of claim 7, further comprising a top metal on top of the bottom die and underneath the insulating material and a portion of the metal, wherein a source metal is not under the bond pad portion of the metal layer.

12. A semiconductor package comprising:

first and second die stacks, each of which includes a bottom die,

a top die, and

a metal layer disposed upon the bottom die, the metal layer being isolated from the bottom die by insulating material, wherein the metal layer acts as a die pad for the top die and as a bond pad for conductive interconnections, and wherein said bottom die is a low side MOSFET and said top die is a high side MOSFET.

13. The package of claim 12, wherein the first and second dies stacks are connected in parallel.

14. The package of claim 12, wherein the first and second die stacks form a full bridge circuit.

15. A method of stacking two discrete dies, comprising:

providing a metal layer on the top of a bottom die, the metal layer being electrically isolated from the bottom die by insulating material;

conductively attaching the bottom of a top die to the metal layer;

routing a connection from the bottom of the top die using the metal layer; and

wherein the bottom die is a first MOSFET having a source on its top and a drain on its bottom, wherein the metal layer is isolated from said source of said first MOSFET by insulating material, and wherein the top die is a second MOSFET having its source contact on its top and a drain contact disposed on its bottom, said drain contact of said second MOSFET being attached to said metal layer.

16. A method of stacking two discrete dies, comprising:

providing a metal layer on the top of a bottom die, the metal layer being electrically isolated from the bottom die by insulating material;

conductively attaching the bottom of a top die to the metal layer;

routing a connection from the bottom of the top die using the metal layer;

placing a source contact on top of the bottom die such that it is underneath the insulating material and a first portion of the metal layer, but not under a portion of the metal layer used for bonding conductive interconnections; and

wherein the discrete semiconductor devices are MOSFETs.

17. The method of claim **15**, wherein the bottom die is a low side MOSFET, and the top die is a high side MOSFET.

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